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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,796	03/23/2001	Paul E. McKenney	BEA9-2001-0001-US1	5819

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LIEBERMAN & BRANDSDORFER, LLC
12221 MCDONALD CHAPEL DRIVE
GAITHERSBURG, MD 20878

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,796	MCKENNEY, PAUL E.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

at page 7, line 26, ",or by inserting special assembly language instructions" is redundant and should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Hagersten (U.S. Patent No. 5,749,095), hereafter referred to as Hagersten'095.

Referring to claims 1 and 12, Hagersten'095 discloses as claimed a method for maximizing CPU performance in a multiprocessor (see Figs. 1 or 2), comprising: (a) allowing local memory (18A or 18B, see Fig. 2) operations to execute in an arbitrary order (since the cache L2 (18A) is individually and locally used by the associated processor 16A, see Fig. 2; and a full associative replacement algorithm certainly is used for cache L2 to have a arbitrary ordering the address of a cache line when required); and (b) providing execution constraints for shared memory (memory 56, see Fig. 1) operations (since the shared memory 56 is controlled by data controller (DC 54) through system interface logic 62, see Col. 12, lines 5-25, regarding the control of write transactions when two nodes performing a transaction to an address).

As to claims 2, 13, and 23, Hagersten'095 also discloses: assigning first and second registers of a CPU for storing associated first and second instruction addresses (note the Hagersten'095's processor 16 certainly comprises registers such as PC (program counter), MAR (memory address register) or CAR (control address register for storing instruction addresses).

As to claim 3, Hagersten'095 also discloses: providing a third instruction referencing said registers (this is the situation when the registers, such as PC (program counter), MAR

(memory address register) or CAR (control address register) storing the first and second instruction addresses is referred to such as the source or destination register in a third instruction).

As to claims 4 and 14, Hagersten'095 also discloses: said third instruction specifies ordering between said first and second instructions (this is the situation when the registers storing the first and second instruction addresses are referred to as the destination register in such as a third LOAD instruction, therefore operating the ordering between said first and second instructions).

As to claims 5 and 15, Hagersten'095 also discloses: said third instruction indicates said first instruction's execution attaining a first specified state of execution prior to said second instruction's execution attaining a second specified state of execution (note this occurs when either one of the first instruction and the second instruction depends from the other).

As to claims 6 and 16, Hagersten'095 also discloses: said first and said second specified states of execution are selected from the group consisting of: committing instruction execution, initiating memory access, completing a memory access, initiating an I/O access, completing an 1/0 access, and completing

instruction execution (note this occurs when the first instruction and the second instruction is a memory load/store operation and it therefore certainly involves at least one of initiating memory access, completing a memory access, initiating as claimed).

As to claims 7, 17, and 24, Hagersten'095 also discloses: assigning a sequence number to an associated instruction for maintaining instruction ordering (note this is the situation in the Hagersten'095's system when a sequence of program is executed such as a logical address or physical address numbers)

As to claims 8 and 18, Hagersten'095 also discloses: statically encoding said sequence number within said instruction (inherently existing in the processor 16 when a sequence of program is therein).

As to claims 9 and 19, Hagersten'095 also discloses: dynamically encoding said sequence number within said instruction (as set forth above, inherently the processor 16 comprises registers such as MAR (memory address register) or CAR (control address register for storing instruction addresses and for dynamically encoding the sequence number).

As to claims 10 and 20, Hagersten'095 also discloses: placing a range of instructions into a hierarchical ordering system (note the control unit of the Hagersten'095's CPU is

reasonably and broadly interpreted as a hierarchical ordering system and a range of instructions is inherently placed in a process table).

As to claims 11, 21 and 25, Hagersten'095 also discloses: implementing a special instruction for maintaining a hierarchical execution of said instruction (such as a microinstruction existing in the processor 16 for control the instruction execution which is broadly interpreted as a special instruction for maintaining a hierarchical execution).

Referring to claim 22, Hagersten'095 discloses as claimed a processor for use in a multiprocessor computer system (see Fig. 2), comprising: a first instruction for allowing local memory (L2, 18A and 18B, see Fig. 2) operations to occur in an arbitrary order (since the cache L2 is individually used by the associated processor 16, see Fig. 2; and a full associative replacement algorithm certainly is used for cache L2), a second instruction for providing shared memory (56, see Fig. 2) operation constraints (note the above limitations are disclosed by Hagersten'095 as set forth above in claim 1); a third instruction for managing order of execution of said first and second instructions (note the above limitations are disclosed by Hagersten'095 as set forth above in claim 4); wherein execution of said second instruction is responsive to said first

instruction reaching a specified state of execution and said specified state of execution is selected from the group consisting of: committing instruction execution, initiating memory access, completing a memory access, initiating an I/O access, completing an 1/0 access, and completing instruction execution (note the above limitations are disclosed by Hagersten'095 as set forth above in claims 5 and 6).

Response to Arguments

4. Applicant's arguments filed 8/7/04 have been fully considered but they are not deemed to be persuasive.

Regarding the specification problems, Applicant's response has not completely overcome these objections.

Applicants argue that Hagersten'095 does not show executing local memory operation in an arbitrary order (page 3, lines 14-15). Examiner disagrees with Applicants. As set forth in the art rejections above, Hagersten'095 discloses as claimed a local memory (18A or 18B, see Fig. 2) operations to execute in an arbitrary order since the cache L2 is individually used by the associated processor 16, see Fig. 2; and a full associative

replacement algorithm certainly is used for cache L2 to have a arbitrary ordering the address of a cache line when required.

Applicants also argue that Hagersten'095's items 18A and 18B are external cache not local memory, and item 22 is designated as memory (page 3, last four lines). Examiner disagrees with Applicants. It is well known to one having ordinary skill in the art that a cache is a memory since it can save a cache line. Regarding "external" and "local", as shown in Fig. 2, obviously, inside the left subnode 50A, L2 18A to processor 16A is a local memory. And inside the right subnode 50B, another L2 18A to another processor 16A is a local memory. A external memory can still be interpreted as a local memory once the memory is disposed locally to a processor. Further, item 56 (in Fig. 2) instead of item 22 (in Fig. 1) is referred to as the memory as claimed.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS

of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

7. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

October 3, 2004